

CLAIMS

1. (Currently Amended) A transmitter coupled to at least two single-channel links of a high-bandwidth link, the transmitter comprising:

at least two registers, each associated with a ~~single-channel~~ different single-channel link and each receiving a different portion of user data provided to the transmitter from a module; and

a framer ~~providing~~ adapted to i) provide the user data from the module as a ~~packet plurality of~~ packets, each having a packet delineator and based on a packet format, and ii) ensure that the packet delineator of each packet is provided on a particular single-channel link; and

wherein one register provides a portion of ~~the~~ each packet with the packet delineator to ~~[[a]]~~ the particular single-channel link, and each register provides a corresponding portion of ~~the~~ each packet to an associated single-channel link.

2. (Original) The invention as recited in claim 1, wherein, for a sequence of packets, the transmitter inserts inter-packet fill to provide the packet delineator of each packet on the particular single-channel link.

3. (Original) The invention as recited in claim 1, wherein at least one single-channel link is a serial link.

4. (Original) The invention as recited in claim 3, wherein the serial link is an 8B/10B encoded link operating in accordance with either a Ethernet standard, a Fibre-channel standard, or a Infiniband standard.

5. (Currently Amended) The invention as recited in claim 3, wherein the serial link applies scrambling to ~~the~~ each packet including the user data.

6. (Original) The invention as recited in claim 3, wherein the serial link operates in accordance with a SONET standard.

7. (Original) The invention as recited in claim 1, wherein the at least two single-channel links are parallel links.

8. (Original) The invention as recited in claim 7, wherein the parallel links operate in accordance with either a PCI bus standard or a RapidIO standard.

9. (Original) The invention as recited in claim 1, wherein the transmitter operates in a node in accordance with an asynchronous transfer mode standard or a synchronous optical network standard.

1 10. (Original) The invention as recited in claim 1, wherein the transmitter is embodied in an
2 integrated circuit.

1 11. (Currently Amended) A receiver generating user data for a module from a ~~packet~~
2 plurality of packets received from at least two single-channel links forming a high-bandwidth link, the
3 receiver comprising:

4 at least two registers, each receiving a different portion of ~~the~~ each packet, wherein

5 one register provides a portion of ~~the~~ each packet with a packet delineator from a
6 particular ~~single-channel~~ single-channel link, and each register provides a corresponding portion
7 of ~~the~~ each packet from an associated single-channel link; and

8 a framer that 1) forms ~~the~~ each packet from ~~the~~ a corresponding packet delineator and 2) extracts
9 the user data based on a packet format.

1 12. (Original) The invention as recited in claim 11, wherein the packet format includes
2 information in at least one message channel other than the user data.

1 13. (Original) The invention as recited in claim 11, wherein the packet format includes error
2 detection or error detection/correction information.

1 14. (Original) The invention as recited in claim 13, wherein the error detection or error
2 detection/correction information is cyclic redundancy check information.

1 15. (Original) The invention as recited in claim 11, wherein the packet format allows for
2 discarding of inter-packet fill.

1 16. (Original) The invention as recited in claim 11, wherein the apparatus operates in a node
2 in accordance with an asynchronous transfer mode standard or a synchronous optical network standard.

1 17. (Original) The invention as recited in claim 11, wherein the circuit is embodied in an
2 integrated circuit.

1 18. (Currently Amended) A method of transmitting user data from a module over at least
2 two single-channel links of a high-bandwidth link, the method comprising the steps of:

3 (a) receiving, in each of at least two registers, each having a corresponding ~~single-channel~~ single-
4 channel link, a different portion of user data from the module; ~~and~~

5 (b) providing ~~1)~~ the user data as a ~~packet~~ plurality of packets, each having a packet delineator and
6 based on a packet format; ~~[[,]]~~ and

7 (c) ~~2)~~ ensuring that the packet delineator of each packet is provided on a particular single-channel
8 link; and

9 wherein one register provides a portion of ~~the~~ each packet with the packet delineator to ~~[[a]]~~ the
10 particular single-channel link, and each register provides a corresponding portion of ~~the~~ each packet to an
11 associated single-channel link.

1 19. (Original) The invention as recited in claim 18, wherein step (b) further includes the step
2 of inserting inter-packet fill such that the packet delineator occurs on the particular single-channel link for
3 each packet in a sequence of packets.

1 20. (Original) The invention as recited in claim 18, wherein, for step (b) at least one single-
2 channel link is a serial link.

1 21. (Original) The invention as recited in claim 20, wherein, for step (b) the serial link is an
2 8B/10B encoded link operating in accordance with either a Ethernet standard, a Fibre-channel standard, or
3 a Infiniband standard.

1 22. (Currently Amended) The invention as recited in claim 20, further including the step of
2 scrambling at least one portion of ~~the~~ each packet including the user data.

1 23. (Original) The invention as recited in claim 20, wherein, for step (b), the serial link
2 operates in accordance with a SONET standard.

1 24. (Original) The invention as recited in claim 18, wherein, for step (b) the at least two
2 single-channel links are parallel links.

1 25. (Original) The invention as recited in claim 18, wherein, for step (b) the parallel links
2 operate in accordance with either a PCI bus standard or a RapidIO standard.

1 26. (Original) The invention as recited in claim 18, wherein the method is implemented
2 within a node in accordance with an asynchronous transfer mode standard or a synchronous optical
3 network standard.

1 27. (Original) The invention as recited in claim 18, wherein the method is implemented
2 within a processor of an integrated circuit.

1 28. (Currently Amended) A method of generating user data for a module from a ~~packet~~
2 plurality of packets received from at least two single-channel links forming a high-bandwidth link, the
3 method comprising the steps of:

4 (a) receiving, in each of at least two registers, a corresponding portion of ~~the~~ each packet;

5 (b) providing a different portion of ~~the~~ each packet with a packet delineator from a particular
6 ~~single-channel~~ single-channel link, and 2) a corresponding portion of each ~~the~~ packet from an associated
7 single-channel link;

8 (c) forming ~~the~~ each packet from ~~the~~ a corresponding packet delineator; and

9 (d) extracting the user data based on a packet format.

1 29. (Original) The invention as recited in claim 28, wherein step (d) extracts information in
2 at least one message channel other than the user data.

1 30. (Currently Amended) The invention as recited in claim 28, wherein step (c) forms ~~the~~
2 each packet based on error detection or error detection/correction information included with the packet in
3 accordance with the packet format.

1 31. (Original) The invention as recited in claim 30, wherein the error detection or error
2 detection/correction information is cyclic redundancy check information.

1 32. (Original) The invention as recited in claim 28, wherein step (c) discards inter-packet
2 fill.

1 33. (Original) The invention as recited in claim 28, wherein the method is implemented
2 within a node in accordance with an asynchronous transfer mode standard or a synchronous optical
3 network standard.

1 34. (Original) The invention as recited in claim 28, wherein the method is implemented
2 within a processor of an integrated circuit.

3 35. (New) The invention as recited in claim 1, wherein the transmitter is adapted to provide
4 the packet delineator of each packet to the particular single-channel link independent of the sizes of the
5 packets.

6 36. (New) The invention as recited in claim 11, wherein the receiver is adapted to provide the
7 packet delineator of each packet from the particular single-channel link independent of the sizes of the
8 packets.

1 37. (New) The invention as recited in claim 18, wherein the provision of the portion of each
2 packet with the packet delineator to the particular single-channel link occurs independently of the sizes of
3 the packets.

4 38. (New) The invention as recited in claim 28, wherein the receipt of the portion of each
5 packet with the packet delineator from the particular single-channel link occurs independently of the sizes
6 of the packets.